High-Voltage GaAs Power-HBTs for Base-Station Amplifiers

P. Kurpas, F. Brunner, R. Doerner, B. Janke, P. Heymann, A. Maasdorf, W. Doser*, P. Auxemery**, H. Blanck*, D. Pons**, J. Würfl, and W. Heinrich

Ferdinand-Braun-Institut (FBH), D-12489 Berlin / Germany
*ums GmbH, D-89081 Ulm / Germany
**ums Orsay, F-91404 Orsay Cedex / France

***Abstract* — Base stations require high-power devices operating at bias voltages around 26 V. This paper reports on GaAs HBTs with increased breakdown voltage. Transistors on unthinned wafers deliver 3.2 W at 2 GHz for 27 V bias. 100 Ohms output impedance and 74% PAE make them very attractive for base-station amplifiers.**

I. Motivation

Base stations for second and third-generation cellular networks require high-power amplifiers. GaAs heterobipolar transistors (HBTs) offer both high power-added efficiency (PAE) and good linearity. Therefore, they are increasingly used in cellular-handset power stages in the 2 GHz frequency range. A typical application is the 3V, 1W unit cell.

The situation in base stations is different since higher power is required but, on the other hand, larger bias voltages are available. The new UMTS networks demand for extremely linear power amplifiers, which in turn drives power levels up taking advantage of back-off operation. What one needs is a device unit cell delivering about 10 W at 27 V bias voltage. Furthermore, the resulting output impedance has to be large enough to allow for parallel operation of several cells without degrading combining efficiency.

So far, primary device candidates for this application are LDMOS-FETs, Si-BJTs, and MESFETs. The present LDMOS and BJT devices are limited in frequency around 2.2 GHz, which is sufficient hitherto, but efficiency at this frequency is low. The latter is true for the MESFET as well. Examples at 26 V bias voltage and 2 GHz deliver 5 W at 37% PAE (LDMOS [1]), 6 W at 25% PAE (BJT [2]), or 10 W at 40% PAE (MESFET [3]).

AlGaAs/GaAs HBTs with good power handling capabilities at bias voltages as high as 28 V were reported in [4]. Applying a special mounting scheme, 20 W cw output power were achieved. This demonstrates the potential of the GaAs HBT for high-voltage applications. But, development of such power cells still remains a demanding task. In a recent contribution [5], 20 V bias voltage with unballasted transistors were achieved.

In this paper, we report on GaInP/GaAs HBT power-cells including emitter ballasting, which can be operated at bias voltages up to 27 V. Results of on-wafer power measurements, although so far on unthinned wafers without heat sinking, demonstrate excellent performance.

II. Technology

A. High-voltage Issues

Key to the desired 25 V bias-voltage operation are high values of collector-base (BV_{cbo}) and collector-emitter breakdown voltage (BV_{ceo}). This is achieved by increasing collector thickness as well as reducing collector doping. Large collector thicknesses mean high topology and lead to technological problems. Collector doping, on the other hand, is limited by background effects and epitaxial growth conditions. Therefore, bearing in mind the tradeoff between these limitations and processing efforts, a collector thickness of 2.8 µm and a minimum doping of $n = 4 \times 10^{15}$ cm^{-3} were chosen.

Moreover, in order to ensure thermal stability and to prevent gain collapse due to current concentration on single fingers, appropriate ballasting is mandatory (see [6]). This is realized in the emitter by introducing a 300 nm low-doped $Ga_{0.51}In_{0.49}P$ layer.

B. Process

The epitaxial layers are grown on 4-inch GaAs substrates by MOVPE. The structure mainly consists of a 700 nm GaAs subcollector layer ($n = 5 \times 10^{18}$ cm^{-3}), a 2800 nm thick GaAs collector layer (doping variation $n = 4...20 \times 10^{15}$ cm^{-3}), a 100 nm GaAs base layer ($p = 4 \times 10^{19}$ cm^{-3}), a 40 nm $Ga_{0.51}In_{0.49}P$ emitter layer ($n = 5 \times 10^{17}$ cm^{-3}), a 300 nm $Ga_{0.51}In_{0.49}P$ ballasting layer, and GaAs and InGaAs contact layers. Si and C are used for the n-type and p-type doping, respectively.

HBT processing is based on a two-mesa approach. Device isolation is realized by He-ion implantation through the subcollector layer. The lateral emitter and base defini-

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tion is based on a combined selective dry and wet-etching process. $WSiN_x$/Ti/Pt/Au, Ti/Pt/Au, and Ni/Ge/Au/Ni/Au metal systems are used for the emitter, base, and collector contacts, respectively.

For interconnections, Ti/Pt/Au metal is used. Emitter thermal shunts consisting of a 20 µm thick electroplated Au-layer are added [7] in order to improve thermal stability and to minimize thermal run-away.

For the etching of the very thick collector layer, which has three times the thickness as compared with the common low-voltage HBTs, sulfuric acid is used taking advantage of its superior selectivity against a 20 nm thin GaInP etch-stop layer. After the collector wet-etching the total topology of the HBT device reaches 4 µm. This requires optimized processing to cope with. We found that after only slight adaptations our thick-resist stepper-lithography is able to provide the required resolution. Therefore, it was not necessary to include any planarization. We use only a 300 nm thin SiN_x layer for passivation.

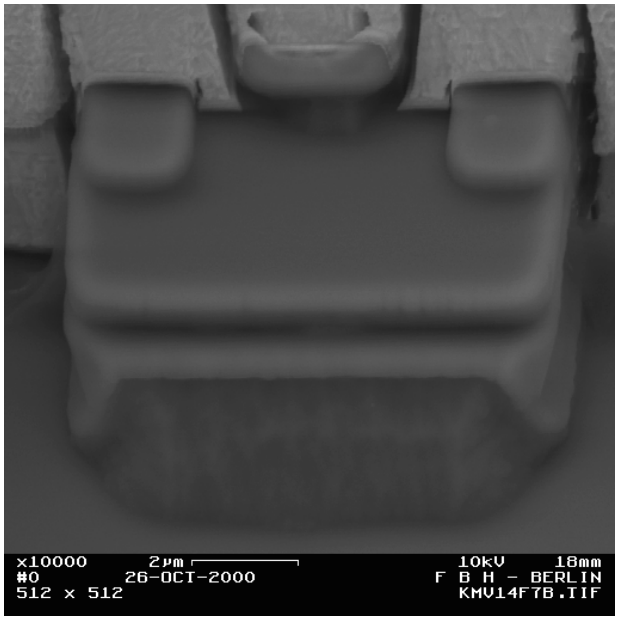

Fig. 1 SEM detail of high-voltage HBT device. The 2.8 µm high collector mesa, the base-contact fingers, and the emitter mesa and metalization can be seen. Also, SiN_x passivation layer and emitter interconnect metal are visible.

C. Device Layout

The emitter size of the HBTs is 3x30 μm^2 per finger. Single-finger devices as well as power cells with up to 10 emitter fingers and a total emitter area of 10x3x30 μm^2 were fabricated. Fig. 2 shows the 10-finger HBT. The 20 µm thick airbridges shunting the emitter fingers thermally and electrically are clearly visible.

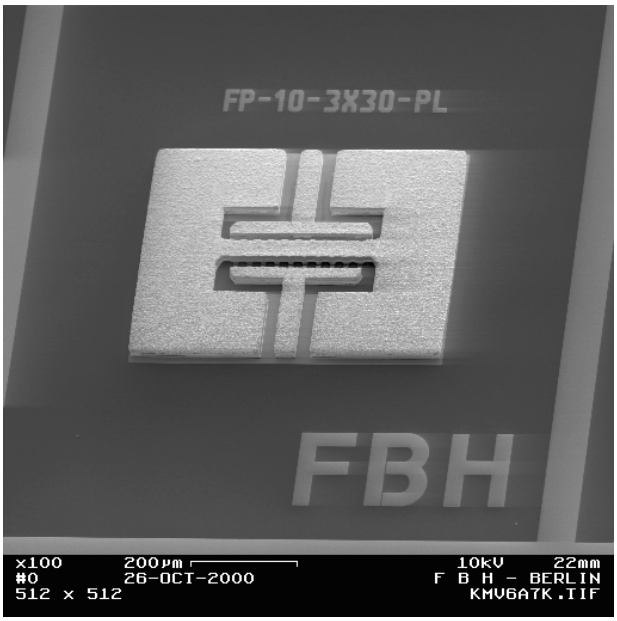

Fig. 2 SEM picture of HBT power cell with 10 emitter fingers (10x3x30 μm^2).

III. MEASUREMENTS

DC measurements are performed using a commercial wafer mapping system. The power performance is characterized by S-parameter and load-pull measurements at 2 GHz (for measurement set-up see [8]). All measurement results presented in the following are on-wafer data referring to the unthinned 625 µm thick wafer. The transistors are probed in a coplanar environment without via-holes or heat sinking. This arrangement provides basic information on the devices and allows comparison to conventional structures. For a full exploitation of their high-power capabilities, of course, thermal management must be improved, e.g., by thinning and appropriate backside processing.

Fig. 3 presents the I-V characteristics of a 10x3x30 μm^2 HBT with 6 x 10^{15} cm^{-3} collector doping. This device is capable to deliver high power at current densities in the range of 2...5 x 10^4 A/cm^{-2}. The behavior resembles that of our standard HBT structures with 1 µm thick collector layer. Important is that the maximum allowable collector current decreases with growing collector-emitter bias voltage. Violating this condition leads to the destruction of the device. The desired voltage values above 20 V can be reached at current densities below 1 x 10^4 A/cm^{-2}.

This strong dependence of the device destruction on bias voltage and current density is obviously caused by the onset of current crunching and rapid thermal runaway of the device. In fact, this explanation correlates well with the observation that always the inner, i.e., the hottest, emitter fingers were destroyed. Further increase of the usable current density at a given collector-emitter voltage can be expected after improvement of the thermal stabilization by appropriate heat sinking.

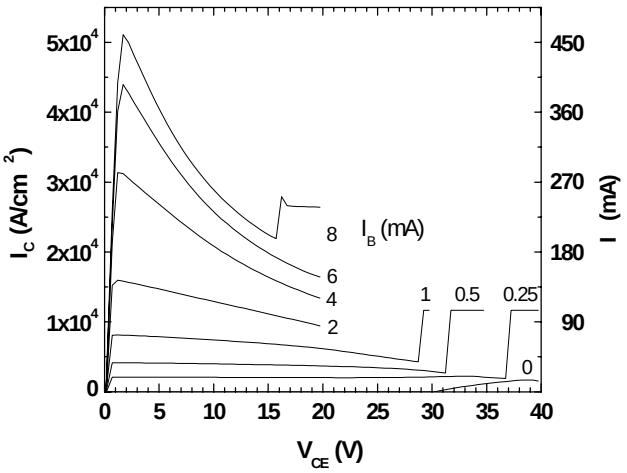

Fig. 3 I-V characteristics of 10 emitter finger HBT (10x3x30 µm^2) with base current I_B as parameter.

S-parameter measurements yield f_T values of 24 GHz and f_{max} values above 50 GHz for a single-finger 1x3x30 µm^2 HBT with a collector doping of 6 x 10^{15} cm^{-3}. The onset of Kirk effect is observed when the collector current density exceeds 2 x 10^4 A/cm^2. For 10 finger devices, f_{max} reduces to about 40 GHz, which is still sufficient for operation up to X band.

Fig. 4 presents on-wafer load-pull measurements of a 10x3x30 µm^2 HBT with 6 x 10^{15} cm^{-3} collector doping. At a collector-emitter bias voltage of 27 V, this device delivers an output power P_{out} of 3.2 W at 74% PAE without harmonic tuning.

What is equally important is the load-impedance level, which reaches 100 Ohms at the fundamental frequency (|r| = 0.51, φ = 36°, corresponding to Z = 85 + j69 Ω with |Z| = 109 Ω). This relatively high value enables simple matching or combining of the cells. It means, for instance, that three of these cells in parallel yield 10 W power at an impedance level of 30 Ohms, which can easily be matched to a 50 Ohm output or used to set up even larger cells. For comparison, the load impedance of the LDMOS-FET [1] at 1.95 GHz, 26 V and 5 W is as low as 7 Ohms.

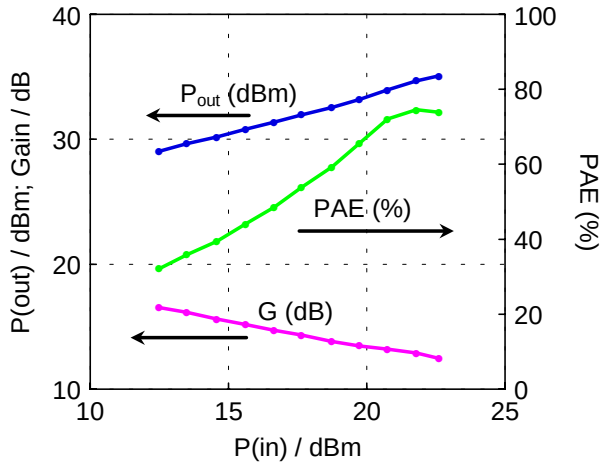

Fig. 4 Output power P(out), gain G, and PAE against input power P(in) for a 10-finger HBT with 10x3x30 µm^2 emitter size at 27 V collector-emitter bias voltage (on-wafer load-pull measurements at 2 GHz without harmonic tuning).

The load-pull measurement set-up [8] is based on a microwave transition analyzer and thus yields not only power data, but also the time dependence of the voltages and currents. This is very helpful for optimization since it provides insight into the actual time-dependent voltages and currents at the transistor. As an example, Fig. 5 presents the time functions of voltage and current at the collector.

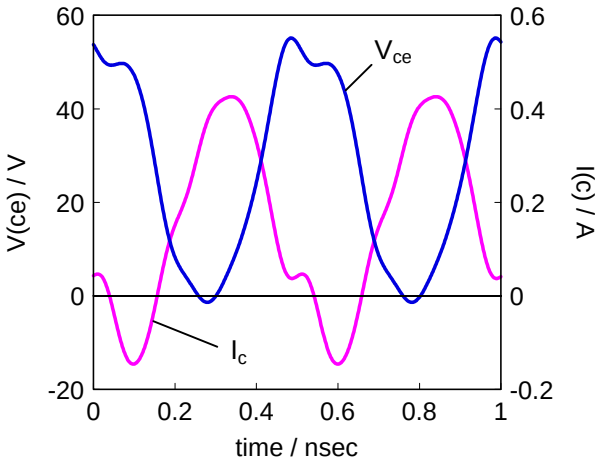

Fig. 5 Collector current I_C and voltage V_{CE} as a function of time (measurements on the load-pull set-up [8] using the microwave transition analyzer, other parameters as in Fig. 4).

IV. CONCLUSIONS

HBTs with high breakdown voltage for high-voltage operation were developed, which show excellent power capabilities. Relatively small 10-finger devices of 10x3x30 μm^2 emitter size could be operated safely at 27 V collector-emitter bias on unthinned wafer without heat sinking. They deliver 3.2 W of microwave power with a PAE of 74% at 2 GHz. These are very promising results since further improvements can be expected when applying appropriate heat sinking techniques.

ACKNOWLEDGEMENT

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